Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1. (*Currently Amended*) A decoder for decoding encoded data, the decoder comprising:

a processor having an input which receives probability estimates for a block of symbols, and which is arranged to calculate probability estimates for said symbols in a next iterative state;

~~normalising means which normalises said next states~~ normalizing means for normalizing said calculated probability estimates to provide normalized probability estimates;

a switch ~~that receives both said normalised and said unnormalised next state~~ arranged to receive both said calculated probability estimates and said normalized probability estimates, [[the]] an output of the switch being coupled to the input of the processor;

wherein the switch is arranged to switch between the ~~normalised and unnormalised next state~~ calculated probability estimates and the normalized probability estimates depending on the iterative state.

Claim 2. (*Currently Amended*) [[A]] The decoder according to claim 1 wherein said decoder comprises a MAP algorithm wherein the probability estimates are α and β values.

Claim 3. (*Currently Amended*) [[A]] The decoder according to claim 1 wherein said decoder has eight iterative states for each received symbol block.

Claim 4. (*Currently Amended*) [[A]] The decoder according to claim 1 wherein the ratio between said ~~unnormalised and said normalised next state~~ calculated probability estimates and said normalized probability estimates is 7:1.

Claim 5. (*Currently Amended*) [[A]] The decoder according to claim 1 wherein said switch is a multiplexer.

Claim 6. (*Currently Amended*) [[A]] The decoder according to claim 1 further comprising pipeline registers between said processor and said ~~normalising~~ normalizing function.

Claim 7. (*Currently Amended*) A turbo decoder comprising [[a]] the decoder according to claim 1.

Claim 8. (*Currently Amended*) A decoder for decoding encoded data, the decoder comprising:

a processor having an input which receives probability estimates for a block of symbols, and which is arranged to calculate probability estimates for said symbols in a next iterative state;

~~normalising~~ normalizing means coupled to the processor ~~which normalises said next state~~ for normalizing said calculated probability estimates to provide normalized probability estimates;

~~wherein the decoder further comprises~~ pipelining means between the processor and the ~~normalising~~ normalizing means for providing ~~non-normalised next state~~ non-normalized probability estimates; and

switching means for receiving both said calculated probability estimates and said normalized probability estimates, an output of the switching means being coupled to the input of the processor;

wherein the switching means is arranged to switch between the calculated probability estimates and the normalized probability estimates depending on the iterative state.

Claim 9 (*Canceled*)

Claim 10. (*Currently Amended*) [[A]] The decoder according to claim 8 wherein said pipelining means is a pipeline register coupled between outputs of said processor and inputs of said ~~normalising~~ normalizing means.